REMARKS

This is in response to the Office Action dated April 11, 2005. Pursuant to this amendment, claims 1-10 and 13-19 are pending in the application. Claims 3-10, 13-14 and 16-19 are amended according to the recommendations of the Examiner. Claims 11 and 12 are canceled. Reexamination and reconsideration are respectfully requested.

The Office Action objected to the dependent claims of the application. Applicant amends the pending dependent claims according to the Examiner's suggestion.

The Office Action objects to claim 1 as not being illustrated in the drawings. Applicant respectfully submits that claim 1 is illustrated in exemplary FIG. 5 of the application. As shown in FIG. 5, first and second pull-down transistors TN11 and TN12 are connected in series between C1 and VSSQ. Transistors TN11 and TN12 are respectively controlled by second (IN2) and third (IN3) input signals.

The Office Action objected to claims 13-14 for reciting "third resistors" without reciting first and second resistors. Applicant amends claims 13 and 14 to address this objection.

The Office Action rejects claim 1 as anticipated by U.S. Patent No. 6,366,114 to Liu, et al. (the Liu patent). Applicant respectfully submits that claim 1 distinguishes over the Liu patent because the Liu patent neither teaches nor suggests the first and second pull-down transistors required by claim 1.

The application describes a number of input and output circuits that can implement the JEDEC standard input and output characteristics described in the application. Claim 1 relates for example to the circuit illustrated in FIG. 5, which includes first and second pull-down transistors TN11 and TN12 connected in series. Because TN11 and TN12 are connected in series, the voltage drop between node C1

and the low voltage supply VSSQ is divided between the two transistors, reducing the voltage drop across each transistor and reducing the stress on the transistors. Reducing the stress on the individual pull-down transistors improves the life of the components of the input and output circuitry.

The Liu patent does not describe the use of plural pull-down transistors in series to reduce the stress on the pull-down transistors. Rather, the Liu patent describes an input and output circuit that controls the ramp and slew of the switching transistors to reduce noise. Referring to FIG. 1 of the Liu patent, it can be seen that there is a single pull-down transistor MOS1 and no second transistor in series with MOS1. The Office Action, which discusses claim 1 at page 4, does not identify a second pull-down transistor. None of the art of record suggests modifying the Liu circuitry to include such a second pull-down transistor.

Claim 1 consequently distinguishes over the Liu patent by reciting that: "a first pull-down transistor controlled by a second input signal and a second pull-down transistor controlled by a third input signal are connected in series between said common node and a low-potential power supply." Because the art of record does not describe or suggest a second pull-down transistor, applicant submits that claim 1 and its dependent claims 3-4 distinguish over the art of record and are in condition for allowance.

The Office Action rejects claim 2 as anticipated by the Liu patent. Applicant submits that claim 2 distinguishes over the Liu patent by reciting the presence of a plurality of unit circuits, as defined by claim 2, with the common connecting point of the plurality of unit circuits connected to ***a single*** output terminal. This is not true of the Liu patent in which a single unit circuit is connected to each of the output terminals of the chip.

The application describes a number of input and output circuits that can implement the JEDEC standard input and output characteristics described in the application. Claim 2 relates for example to the circuit illustrated in FIG. 3, which includes first and second unit circuits B1 and B2, each including a pull-up transistor (TP1 and TP2, respectively) and a pull-down transistor (TN1 and TN2, respectively) and each have a common node (C1 and C2, respectively) between their respective pull-up and pull-down transistors connected through a resistor (R11 and R12, respectively) to the ***single*** output terminal (OUT). Because two unit circuits are provided with distinct resistors between the unit circuits and the output terminal, output current variations are reduced and there is greater flexibility in designing the performance of the FIG. 3 circuit.

The Liu patent does not describe the use of plural unit circuits connected to a single output terminal. Rather, the Liu patent describes a single unit circuit having one pull-up transistor and one pull down transistor connected to one output terminal. The Liu patent teaches a single unit circuit that controls the ramp and slew of the pull-up and pull-down transistors to reduce noise. Referring to FIG. 1 of the Liu patent, it can be seen that there is a single pull-up transistor MOS2 and a single pull-down transistor MOS1, with a common node connected through a single resistor R3 to the output terminal OUT. Because the Liu patent provides only a single unit circuit for each output terminal OUT of the chip. None of the art of record suggests modifying the Liu patent's circuitry to include a second unit circuit for an output terminal OUT to which a first unit circuit is connected.

Thus, claim 2 distinguishes over the art of record by reciting "an output terminal connected to a common connecting point of said common nodes of said plurality of unit circuits." Claims 5-10 depend from claim 2 and similarly

distinguish over the art of record. Claims 2 and 5-10 are consequently in condition for allowance.

Claims 11 and 12 are canceled.

The Office Action rejects claims 13 and 14 as anticipated by the Liu patent. Applicant submits that claims 13 and 14 distinguish over the Liu patent by reciting the presence of a plurality of unit circuits, as defined by claim 13, with the common connecting point of the plurality of unit circuits connected to ***a single*** output terminal. This is not true of the Liu patent in which a single unit circuit is connected to each of the output terminals of the chip.

The explanation of why the Liu patent does not anticipate or render obvious claim 2 above applies fully here. Thus, claim 13 and its dependent claim 14 distinguish over the Liu patent by reciting "an output terminal connected to a common connecting point of said common nodes of said plurality of unit circuits." The Liu patent does not describe or suggest a plurality of unit circuits connected to a single output terminal and so does not anticipate claim 13 or its dependent claim 14.

The Office Action rejects claims 15-19 as anticipated by U.S. Patent No. 6.737,886 to Curatolo, et al. (the Curatolo patent). The Curatolo patent, like the Liu patent, shows in its FIG. 1 a single unit circuit including two transistors P1, N1 having a common node connected through a resister Rout to an output terminal OUT. The Curatolo patent provides no description of a plurality of unit circuits connected to separate resisters, in turn are connected to a single output terminal, as required by claim 15. Consequently, the Curatolo patent does not anticipate claims 15-19, which recite "first resistors connected respectively between said common nodes of said plurality of unit circuits and a common connecting point of said

common nodes." Claims 15-19 distinguish over the Curatolo patent and the other art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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